
Section 23. Serial Peripheral Interface (SPI)

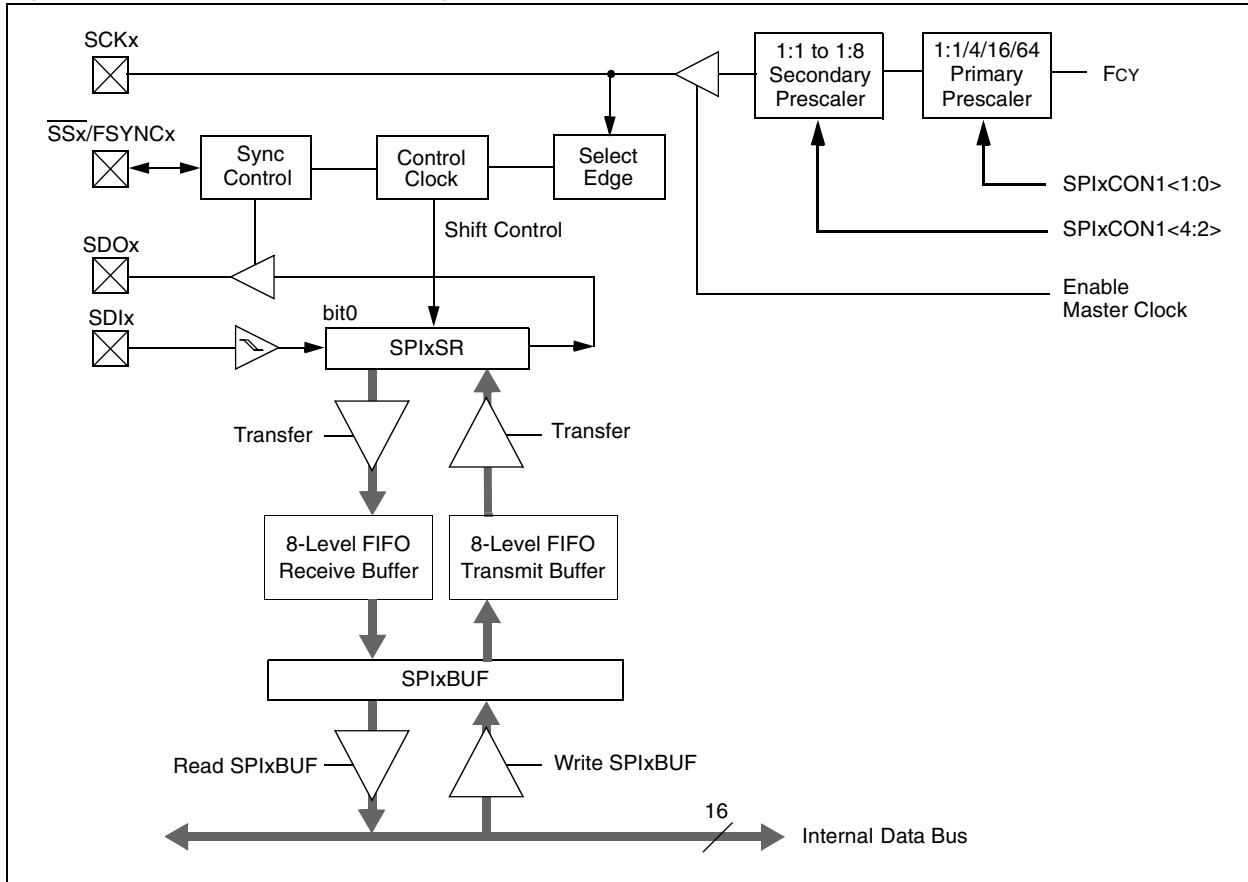
HIGHLIGHTS

This section of the manual contains the following major topics:

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Figure 23-2: SPIx Module Block Diagram (Enhanced Mode)



23.2 STATUS AND CONTROL REGISTERS

The SPIx serial port consists of the following Special Function Registers:

- SPIxBUF: The address in SFR space that is used to buffer data to be transmitted and data that is received (in Standard modes) or to access the FIFO buffer (in Enhanced Buffer modes). This address is shared by the virtual SPIxTXB and SPIxRXB registers.
- SPIxCON1 and SPIxCON2: Control registers that configure the module for various modes of operation.
- SPIxSTAT: A status register that indicates various status conditions.

In addition, a 16-bit shift register, SPIxSR, is used for shifting data in and out of the SPIx port. The shift register is not memory mapped.

23.2.1 SPIxBUF Register

The memory mapped register, SPIxBUF, is the SPIx Data Receive/Transmit register. In Standard modes, the SPIxBUF register is actually comprised of two separate registers: the Transmit Buffer, SPIxTXB, and the Receive Buffer, SPIxRXB. These two unidirectional, 16-bit registers share the SFR address of SPIxBUF. If a user writes data to be transmitted to the SPIxBUF address, internally the data is written to the SPIxTXB register. Similarly, when the user reads the received data from SPIxBUF, internally the data is read from the SPIxRXB register.

When the enhanced buffer is enabled, SPIxBUF becomes the data interface to two 8-level FIFOs: one for reception and another for transmission. Each buffer can hold up to eight pending data transfers. When the CPU writes data to SPIxBUF, the data is moved into the next transmit buffer location. The SPIx peripheral begins to transfer data after the first CPU write to SPIxBUF, and continues until all pending transfers have completed. After each transfer completes, the SPIx updates the next receive buffer location with the received data and is available for the CPU to read. After the CPU read, data is read from the next receive buffer location.

Note: In Standard modes, the SPIxBUF register must not be written before SPIxTBF bit is set. Similarly, the SPIxBUF register must not be read before the SPIxRBF bit is set.

Both modes double-buffer transmit and receive operations and allow continuous data transfers in the background. Transmission and reception occur simultaneously.

23.2.2 Status and Control Registers

The SPIxSTAT and SPIxCON1/SPIxCON2 registers provide the interface to control the module's operation. They are shown in detail in Register 23-1, Register 23-2 and Register 23-3.

Note: SPIxCON1 and SPIxCON2 can not be written while the SPIx modules are enabled. The SPIEN (SPIxSTAT<15>) bit must be clear before modifying either register.

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Register 23-1: SPIxSTAT: SPIx Status Register

| | | | | | | | |
|--------|-----|--------|-----|-----|---------|---------|---------|
| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| SPIEN | — | SPIIDL | — | — | SPIBEC2 | SPIBEC1 | SPIBEC0 |
| Bit 15 | | | | | | | Bit 8 |

| | | | | | | | |
|-------|-----------|--------|--------|--------|--------|-------------|-------------|
| R-0 | R/C-0; HS | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0; HS; HC | R-0; HS; HC |
| SRMPT | SPIROV | SRXMPT | SISEL2 | SISEL1 | SISEL0 | SPIxTBF | SPIxRBF |
| Bit 7 | | | | | | | Bit 0 |

Legend:

R = Readable bit W = Writable bit C = Clearable bit
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown
 HS = Set in Hardware bit HC = Cleared in Hardware bit U = Unimplemented bit, read as '0'

- bit 15 **SPIEN:** SPIx Enable bit
 1 = Enables module and configures SCKx, SDOx, SDIx and \overline{SSx} as serial port pins
 0 = Disables module
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SPIIDL:** Stop in Idle Mode bit
 1 = Discontinue module operation when device enters Idle mode.
 0 = Continue module operation in Idle mode.
- bit 12-11 **Unimplemented:** Read as '0'
- bit 10-8 **SPIBEC2:SPIBEC0:** SPIx Buffer Element Count bits
 Master mode:
 Number of SPIx transfers pending.
 Slave mode:
 Number of SPIx transfers unread.
- bit 7 **SRMPT:** Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode)
 1 = SPIx Shift register is empty and ready to send or receive
 0 = SPIx Shift register is not empty
- bit 6 **SPIROV:** Receive Overflow Flag bit
 1 = New byte/word is completely received; CPU has not read previous data in the SPIBUF register
 0 = No overflow
- bit 5 **SRXMPT:** Receive FIFO Empty bit (valid in Enhanced Buffer mode)
 1 = RX FIFO is empty
 0 = RX FIFO is not empty
- bit 4-2 **SISEL2:SISEL0:** SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)
 111 = Interrupt when SPIx transmit buffer is full (SPIxTBF bit is set)
 110 = Interrupt when last bit is shifted into SPIxSR, as a result, the TX FIFO is empty
 101 = Interrupt when the last bit is shifted out of SPIxSR, now the transmit is complete
 100 = Interrupt when one data is shifted into the SPIxSR, as a result, the TX FIFO has one open spot
 011 = Interrupt when SPIx receive buffer is full (SPIxRBF bit set)
 010 = Interrupt when SPIx receive buffer is 3/4 or more full
 001 = Interrupt when data is available in receive buffer (SRMPT bit is set)
 000 = Interrupt when the last data in the receive buffer is read, as a result, the buffer is empty (SRXMPT bit set)

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Register 23-1: SPIxSTAT: SPIx Status Register (Continued)

- bit 1 **SPIxTBF:** SPIx Transmit Buffer Full Status bit
1 = Transmit not yet started, SPIxTXB is full
0 = Transmit started, SPIxTXB is empty
- Standard Buffer Mode
Automatically set in hardware when core writes SPIxBUF location, loading SPIxTXB.
Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR.
- Enhanced Buffer Mode
Automatically set in hardware when CPU writes SPIxBUF location, loading the last available buffer location.
Automatically cleared in hardware when a buffer location is available for a CPU write.
- bit 0 **SPIxRBF:** SPIx Receive Buffer Full Status bit
1 = Receive complete, SPIxRXB is full
0 = Receive is not complete, SPIxRXB is empty
- Standard Buffer Mode
Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB.
Automatically cleared in hardware when core reads SPIxBUF location, reading SPIxRXB.
- Enhanced Buffer Mode
Automatically set in hardware when SPIx transfers data from SPIxSR to buffer, filling the last unread buffer location.
Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

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Register 23-2: SPIxCON1: SPIx Control Register 1

| | | | | | | | |
|--------|-----|-----|--------|--------|--------|-------|--------------------|
| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE ⁽¹⁾ |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SSEN | CKP | MSTEN | SPRE2 | SPRE1 | SPRE0 | PPRE1 | PPRE0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12 **DISSCK:** Disable SCKx pin bit (SPIx Master modes only)
 - 1 = Internal SPIx clock is disabled, pin functions as I/O
 - 0 = Internal SPIx clock is enabled
- bit 11 **DISSDO:** Disable SDOx Pin bit
 - 1 = SDOx pin is not used by module, pin functions as I/O
 - 0 = SDOx pin is controlled by the module
- bit 10 **MODE16:** Word/Byte Communication Select bit
 - 1 = Communication is word-wide (16 bits)
 - 0 = Communication is byte-wide (8 bits)
- bit 9 **SMP:** SPIx Data Input Sample Phase bit
 - Master mode:
 - 1 = Input data sampled at end of data output time
 - 0 = Input data sampled at middle of data output time
 - Slave mode:
 - SMP must be cleared when SPIx is used in Slave mode.
- bit 8 **CKE:** SPIx Clock Edge Select bit⁽¹⁾
 - 1 = Serial output data changes on transition from active clock state to Idle clock state (see bit 6)
 - 0 = Serial output data changes on transition from Idle clock state to active clock state (see bit 6)
- bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
 - 1 = \overline{SSx} pin used for Slave mode
 - 0 = \overline{SSx} pin not used by module, pin controlled by port function
- bit 6 **CKP:** Clock Polarity Select bit
 - 1 = Idle state for clock is a high level; active state is a low level
 - 0 = Idle state for clock is a low level; active state is a high level
- bit 5 **MSTEN:** Master Mode Enable bit
 - 1 = Master mode
 - 0 = Slave mode
- bit 4-2 **SPRE2:SPRE0:** Secondary Prescale bits (Master mode)
 - 111 = Secondary prescale 1:1
 - 110 = Secondary prescale 2:1
 - ...
 - 000 = Secondary prescale 8:1
- bit 1-0 **PPRE1:PPRE0:** Primary Prescale bits (Master mode)
 - 11 = Primary prescale 1:1
 - 10 = Primary prescale 4:1
 - 01 = Primary prescale 16:1
 - 00 = Primary prescale 64:1

Note 1: The CKE bit is not used in the Framed SPI modes. The user should program this bit to '0' for the Framed SPI modes (FRMEN = 1).

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Register 23-3: SPIxCON2: SPIx Control Register 2

| | | | | | | | |
|--------|--------|---------|-----|-----|-----|-----|-------|
| R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| FRMEN | SPIFSD | SPIFPOL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-------|--------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | — | SPIFE | SPIBEN |
| bit 7 | | | | | | bit 0 | |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 15 **FRMEN:** Framed SPIx Support bit
 1 = Framed SPIx support enabled
 0 = Framed SPIx support disabled

- bit 14 **SPIFSD:** Frame Sync Pulse Direction Control on \overline{SSx} pin bit
 1 = Frame sync pulse input (slave)
 0 = Frame sync pulse output (master)

- bit 13 **SPIFPOL:** Frame Sync Pulse Polarity Control on \overline{SSx} pin bit (Framed modes only)
 1 = Frame sync pulse is active-high
 0 = Frame sync pulse is active-low

- bit 12-2 **Unimplemented:** Read as '0'

- bit 1 **SPIFE:** Frame Sync Pulse Edge Select bit
 1 = Frame sync pulse coincides with first bit clock
 0 = Frame sync pulse precedes first bit clock

- bit 0 **SPIBEN:** Enhanced Buffer Enable bit
 1 = Enhanced Buffer enabled
 0 = Enhanced Buffer disabled (Legacy mode)

23.3 MODES OF OPERATION

The SPIx module has flexible operating modes which are discussed in the following subsections:

- 8-Bit and 16-Bit Data Transmission/Reception
- Master and Slave Modes
- Framed SPI Modes

23.3.1 8-Bit vs. 16-Bit Operation

The MODE16 control bit (SPIxCON1<10>) allows the module to communicate in either 8-bit or 16-bit modes. The functionality will be the same for each mode, except for the number of bits that are received and transmitted. Additionally, the following should be noted in this context:

The module is reset when the value of the MODE16 bit is changed. Consequently, the bit should not be changed during normal operation.

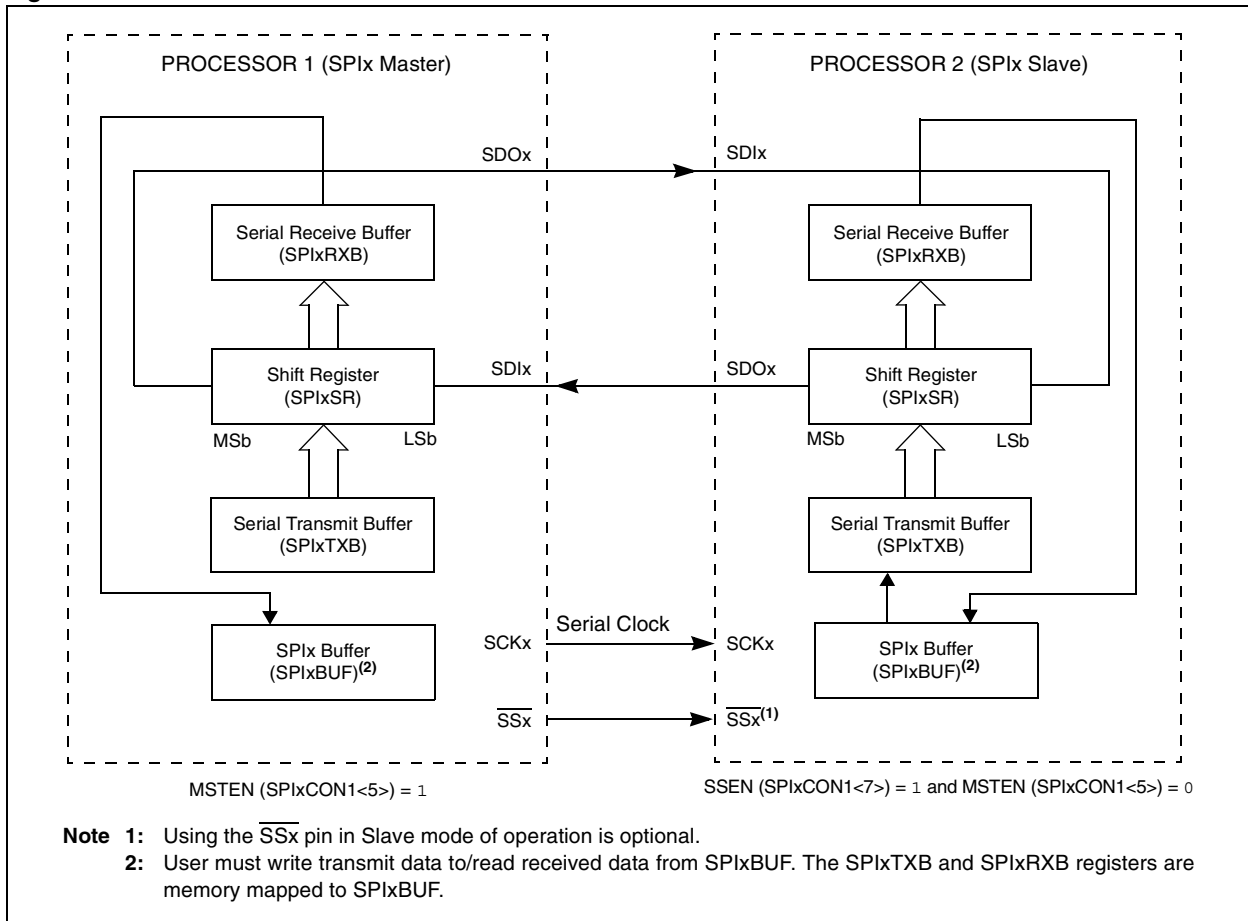
Data is transmitted out of bit 7 of the SPIxSR for 8-bit operation, while it is transmitted out of bit 15 of the SPIxSR for 16-bit operation. In both modes, data is shifted into bit 0 of the SPIxSR.

When transmitting or receiving data, 8 clock pulses at the SCKx pin are required to shift in/out data in 8-bit mode, while 16 clock pulses are required in 16-bit mode.

23.3.2 Master and Slave Modes

In Standard (legacy) Master and Slave modes, data can be thought of as taking a direct path between the Most Significant bit of one module's shift register and the Least Significant bit of the other, and then into the appropriate Transmit or Receive Buffer. The module configured as the master module provides the serial clock and synchronization signals (as required) to the slave device. The relationship between the master and slave modules is shown in Figure 23-3.

Figure 23-3: SPIx Master/Slave Connection



23.3.2.1 MASTER MODE

In Standard Master mode, the system clock is prescaled and then used as the serial clock. The prescaling is based on the settings in the PPRE1:PPRE0 (SPIxCON1<1:0>) and SPRE2:SPRE0 (SPIxCON1<4:2>) bits. The serial clock is output via the SCKx pin to slave devices. Clock pulses are only generated when there is data to be transmitted. For further information, refer to **Section 23.4 “SPI Master Mode Clock Frequency”**. The CKP and CKE bits determine, on which edge of the clock, data transmission occurs.

Both data to be transmitted and data that is received are respectively written into, or read from, the SPIxBUF register.

The following describes the SPIx module operation in Master mode:

1. Once the module is set up for Master mode of operation and enabled, data to be transmitted is written to the SPIxBUF register. The SPIxTBF (SPIxSTAT<1>) bit is set.
2. The contents of SPIxTXB are moved to the Shift register, SPIxSR, and the SPIxTBF bit is cleared by the module.
3. A series of 8/16 clock pulses shifts out 8/16 bits of transmit data from the SPIxSR to the SDOx pin and simultaneously shifts in the data at the SDIx pin into the SPIxSR.
4. When the transfer is complete, the following events will occur:
 - The interrupt flag bit, SPIxIF, is set. SPIx interrupts can be enabled by setting the interrupt enable bit, SPIxIE. The SPIxIF flag is not cleared automatically by the hardware.
 - Also, when the ongoing transmit and receive operation is completed, the contents of the SPIxSR are moved to the SPIxRXB register.
 - The SPIxRBF (SPIxSTAT<0>) bit is set by the module, indicating that the receive buffer is full. Once the SPIxBUF register is read by the user code, the hardware clears the SPIxRBF bit.
5. If the SPIxRBF bit is set (receive buffer is full) when the SPIx module needs to transfer data from SPIxSR to SPIxRXB, the module will set the SPIROV (SPIxSTAT<6>) bit, indicating an overflow condition.
6. Data to be transmitted can be written to SPIxBUF by the user software at any time as long as the SPIxTBF (SPIxSTAT<1>) bit is clear. The write can occur while SPIxSR is shifting out the previously written data, allowing continuous transmission.

Note: The SPIxSR register cannot be written into directly by the user. All writes to the SPIxSR register are performed through the SPIxBUF register.

To set up the SPIx module for the Master mode of operation:

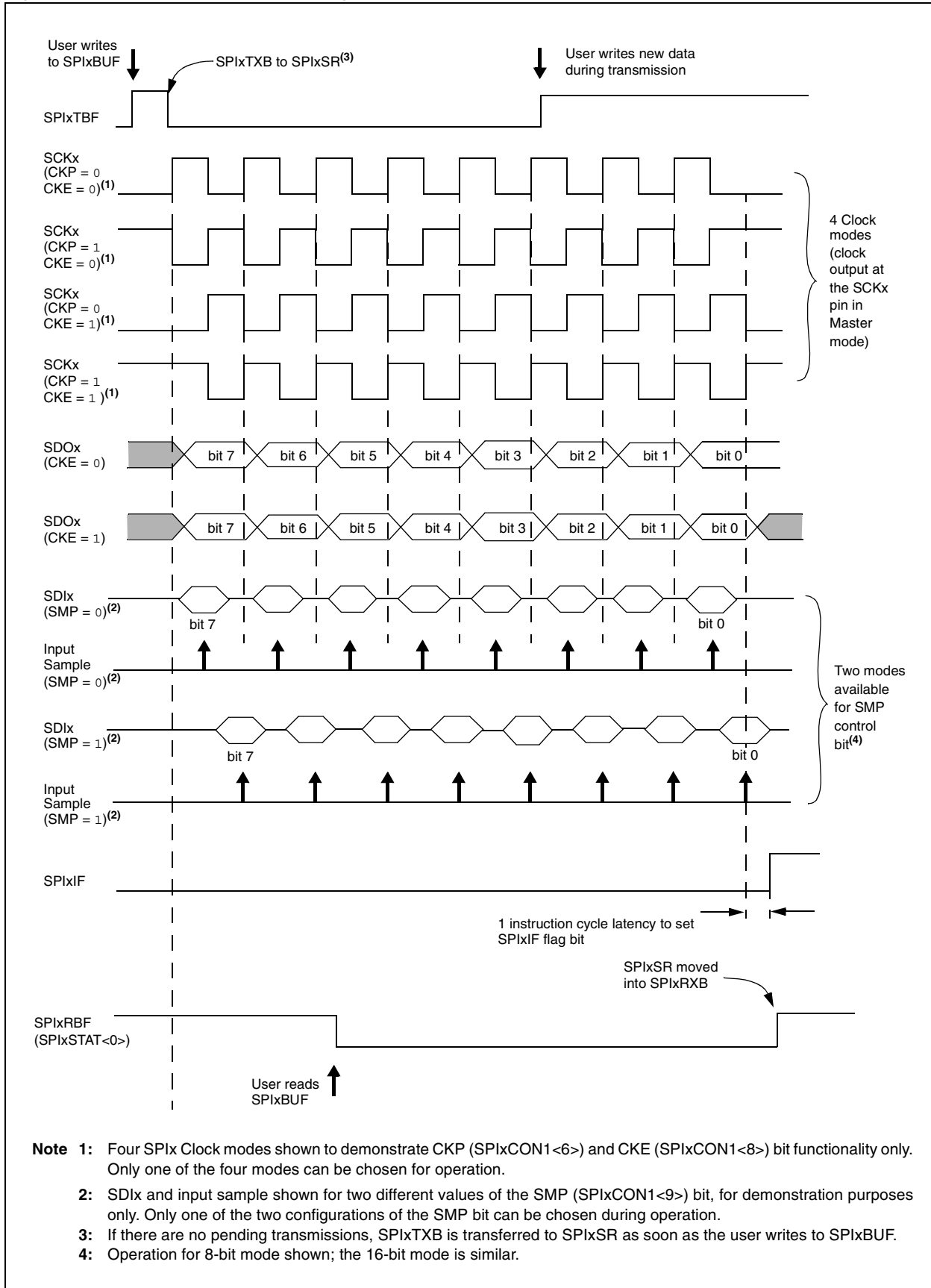
1. If using interrupts:
 - Clear the SPIxIF bit in the respective IFSn register.
 - Set the SPIxIE bit in the respective IECn register.
 - Write the SPIxIP bits in the respective IPCn register to set the interrupt priority.
2. Write the desired settings to the SPIxCON register with MSTEN (SPIxCON1<5>) = 1.
3. Clear the SPIROV bit (SPIxSTAT<6>).
4. Enable SPIx operation by setting the SPIEN bit (SPIxSTAT<15>).
5. Write the data to be transmitted to the SPIxBUF register. Transmission (and reception) will start as soon as data is written to the SPIxBUF register.

23.3.2.1.1 External Clocking in Master Mode

In Standard Master mode, the module can also be configured to operate with an external data clock. SPIx clock operation is controlled by the DISSCK bit (SPIxCON1<12>). When this bit is set, the internal data clock is disabled and data is transferred when external clock pulses are presented on the SCKx pin. All other aspects of Standard Master mode operation are the same as before.

Note: The DISSCK bit is available only in SPI Master modes.

Figure 23-4: SPIx Master Mode Timing



23.3.2.2 SLAVE MODE

In Slave mode, data is transmitted and received as the external clock pulses appear on the SCKx pin. The CKP (SPIxCON<6>) and CKE (SPIxCON<8>) bits determine on which edge of the clock data transmission occurs. Both data to be transmitted and data that is received are respectively written into or read from the SPIxBUF register. The rest of the operation of the module is identical to that in the Master mode.

To set up the SPIx module for the Standard Slave mode of operation:

1. Clear the SPIxBUF register.
2. If using interrupts:
 - Clear the SPIxIF bit in the respective IFSn register.
 - Set the SPIxIE bit in the respective IECn register.
 - Write the SPIxIP bits in the respective IPCn register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1 and SPIxCON2 registers with MSTEN (SPIxCON1<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit is set, then the SSEN bit (SPIxCON1<7>) must be set to enable the \overline{SSx} pin.
6. Clear the SPIROV bit (SPIxSTAT<6>).
7. Enable SPIx operation by setting the SPIEN bit (SPIxSTAT<15>).

23.3.2.2.1 Slave Select Synchronization

The \overline{SSx} pin allows a Synchronous Slave mode. If the SSEN (SPIxCON1<7>) bit is set, transmission and reception are enabled in Slave mode only if the \overline{SSx} pin is driven to a low state (see Figure 23-6). The port output or other peripheral outputs must not be driven in order to allow the \overline{SSx} pin to function as an input. If the SSEN bit is set and the \overline{SSx} pin is driven high, the SDOx pin is no longer driven and will tri-state even if the module is in the middle of a transmission. An aborted transmission will be retried the next time the \overline{SSx} pin is driven low, using the data held in the SPIxTXB register. If the SSEN bit is not set, the \overline{SSx} pin does not affect the module operation in Slave mode.

Note: To meet module timing requirements, the \overline{SSx} pin must be enabled in Slave mode when CKE = 1 (refer to Figure 23-7 for details).

23.3.2.2.2 SPIxTBF Status Flag Operation

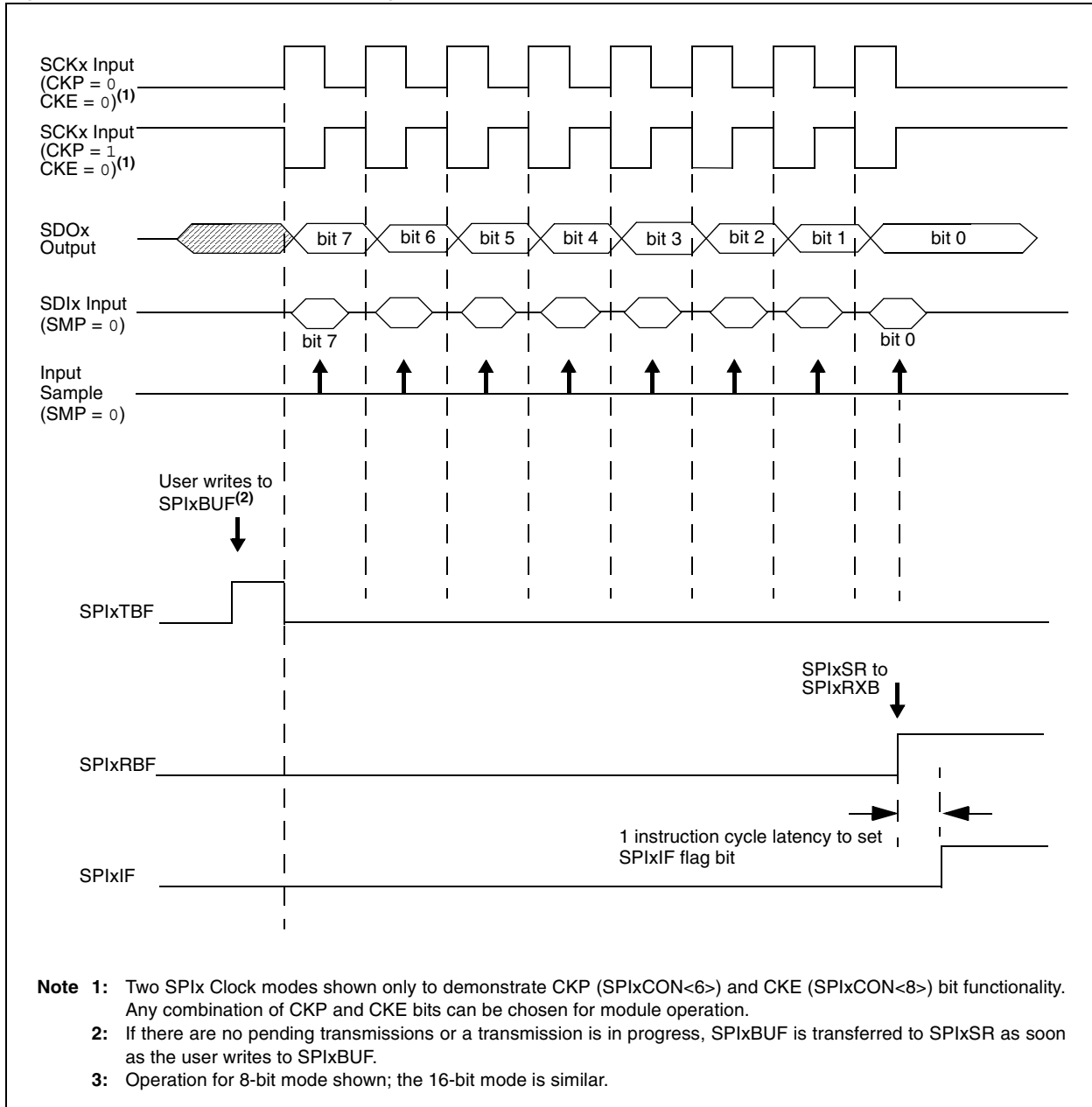
The function of the SPIxTBF (SPIxSTAT<1>) bit is different in the Slave mode of operation.

If SSEN (SPIxCON1<7>) is cleared, the SPIxTBF is set when the SPIxBUF is loaded by the user code. It is cleared when the module transfers SPIxTXB to SPIxSR. This is similar to the SPIxTBF bit function in Master mode.

If SSEN is set, the SPIxTBF is set when the SPIxBUF is loaded by the user code. However, it is cleared only when the SPIx module completes data transmission. A transmission will be aborted when the \overline{SSx} pin goes high and may be retried at a later time. Each data word is held in SPIxTXB until all bits are transmitted to the receiver.

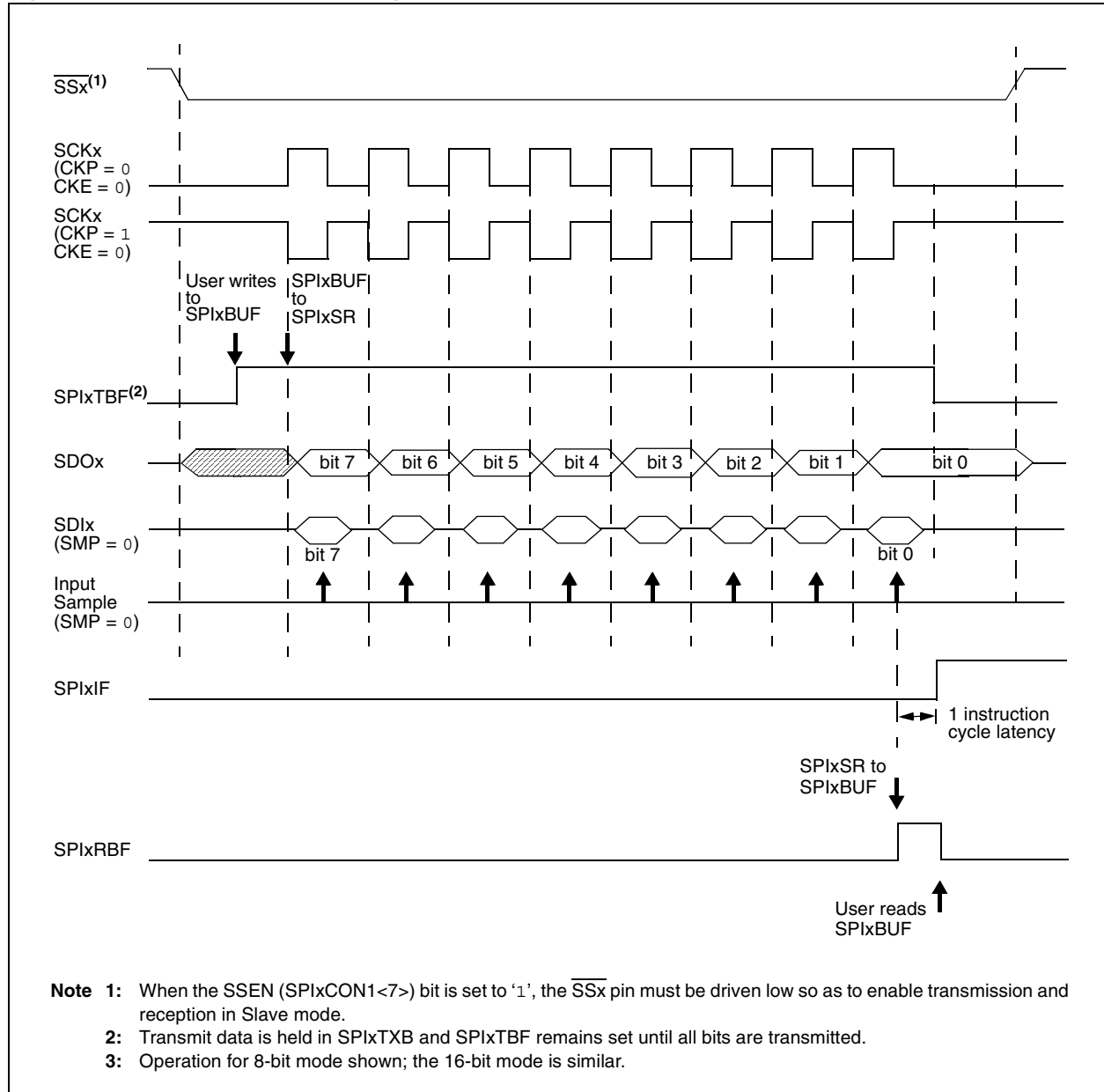
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Figure 23-5: SPIx Slave Mode Timing (Slave Select Pin Disabled)⁽³⁾



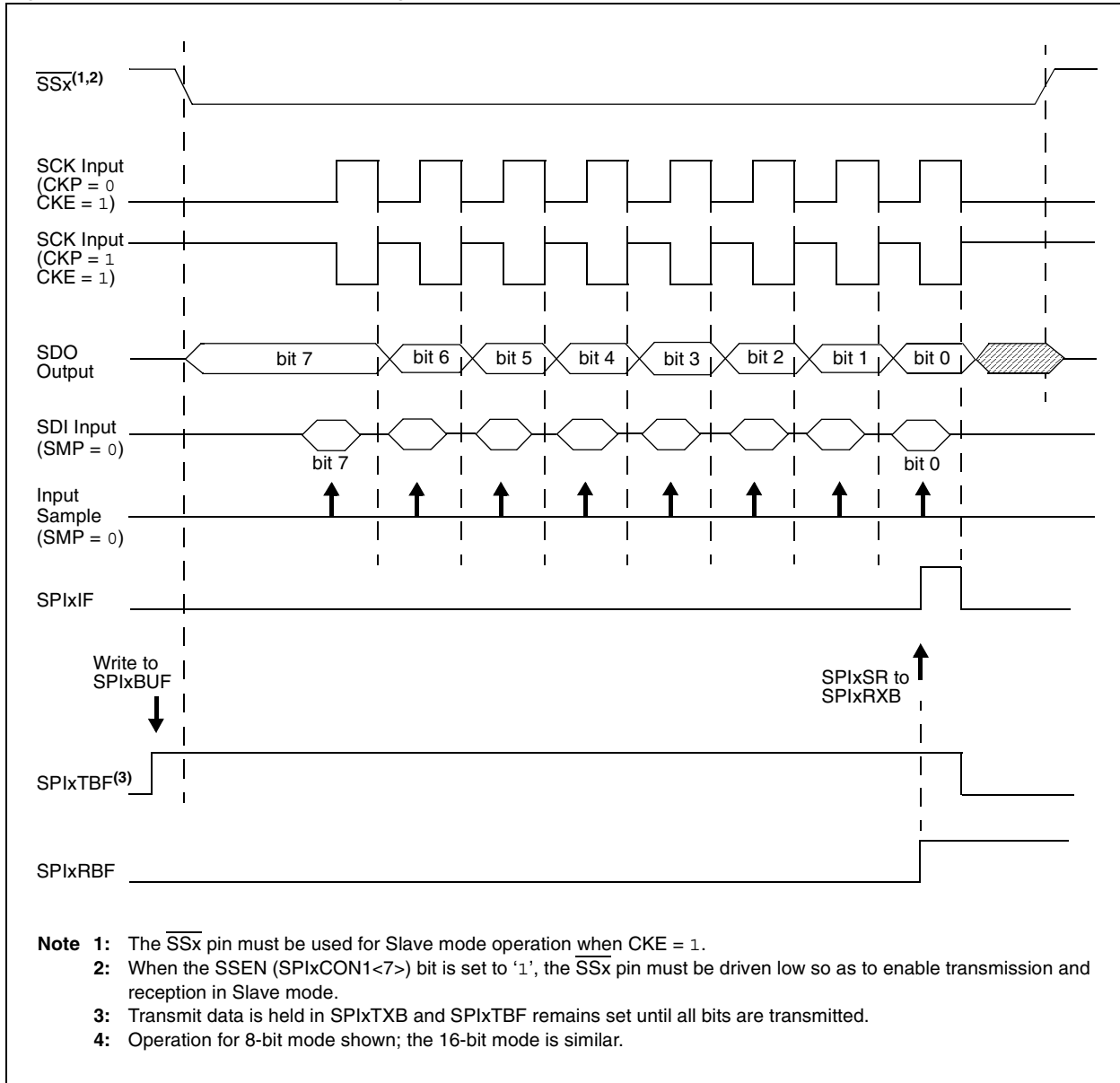
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Figure 23-6: SPIx Slave Mode Timing (Slave Select Pin Enabled)⁽³⁾



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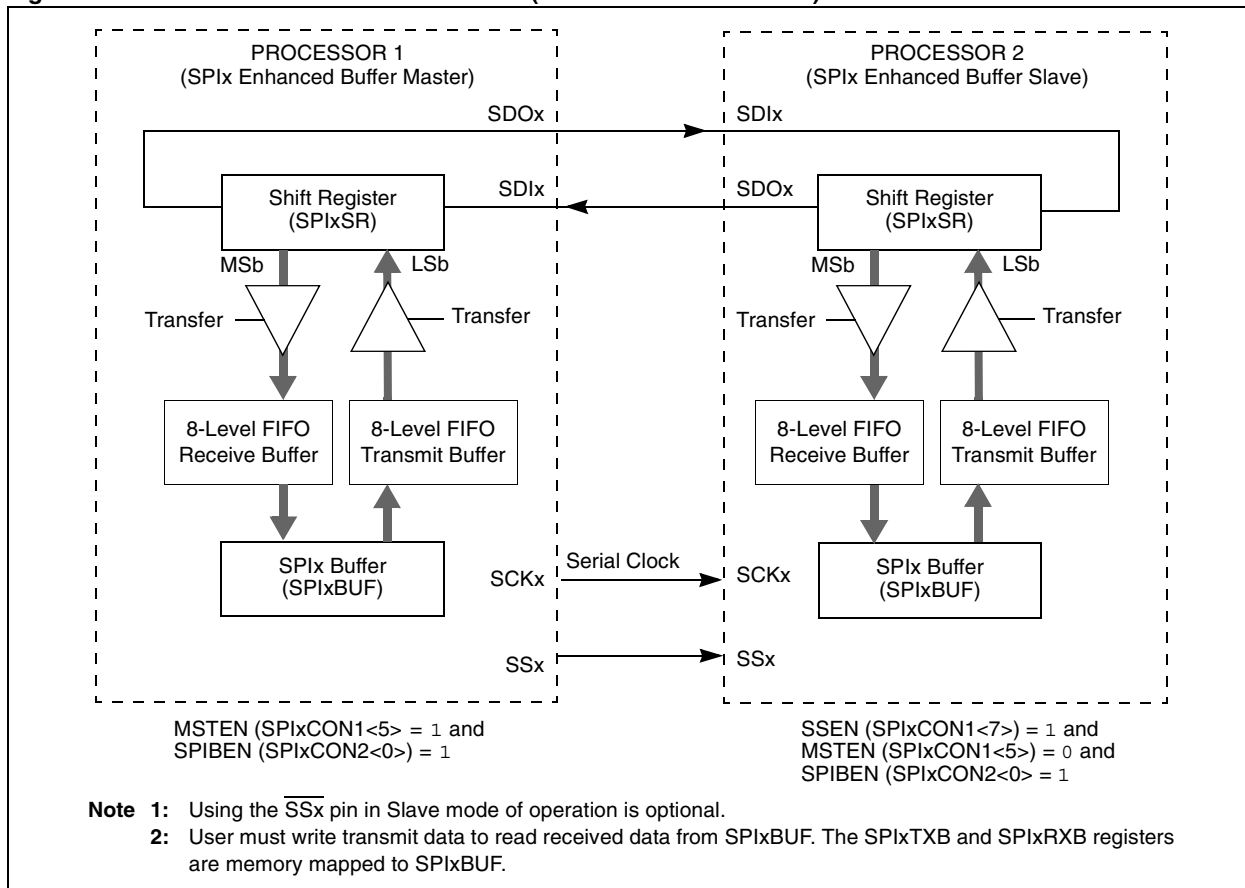
Figure 23-7: SPIx Slave Mode Timing (CKE = 1)⁽⁴⁾



23.3.3 Enhanced Buffer Master and Slave Modes

The operation of Enhanced Buffer Master and Slave modes is very similar to Standard Master and Slave modes. The difference is that data can be thought of as moving from the Shift register to a receive FIFO buffer and moving from the transmit FIFO buffer to the Shift register. The relationships in Enhanced Buffer mode are shown in Figure 23-8.

Figure 23-8: SPIx Master/Slave Connection (Enhanced Buffer Modes)



23.3.3.1 ENHANCED BUFFER MASTER MODE

In Enhanced Buffer Master mode, the system clock is prescaled and then used as the serial clock. The prescaling is based on the settings in the PPRE1:PPRE0 (SPIxCON1<1:0>) and SPRE1:SPRE0 (SPIxCON1<4:2>) bits. The serial clock is output via the SCKx pin to slave devices. Clock pulses are only generated when there is data to be transmitted. For further information, refer to **Section 23.4 “SPI Master Mode Clock Frequency”**. The CKP and CKE bits determine on which edge of the clock, data transmission occurs.

The CPU loads data to be transmitted into the transmit buffer by writing the SSPBUF register. An SPIx transmission begins after the first buffer write. Up to eight pending transmissions can be loaded. The number of pending transfers is indicated by the Buffer Element Count bits SPIBEC2:SPIBEC0 (SPIxSTAT<2:0>).

In Master mode, this count reflects the number of transfers pending in the transmit buffer. In Slave mode, it reflects the number of unread receptions in the receive buffer. If the Shift register is empty, the first write will immediately load the Shift register, leaving 8 transmit buffer locations available.

After an SPIx transfer completes, the receive buffer location is updated with the received data. The CPU accesses the received data by reading the SSPBUF register. After each CPU read, the SSPBUF points to the next buffer location. SPIx transfers continue until all pending data transfers have completed.

The SPIx module follows this sequence in Enhanced Buffer Master mode:

1. Once the module is set up for Master mode of operation and enabled, data to be transmitted is written to the SPIxBUF register and is loaded into the next available transmit buffer location. The SPIxTBF bit (SPIxSTAT<1>) and SPIxIF bit are set after eight pending transfers are loaded.
2. The current buffer location's contents are moved to the Shift register, SPIxSR. The SPIxTBF bit is cleared by the module if a buffer location is available for a CPU write.
3. A series of 8/16 clock pulses shift out 8/16 bits of transmit data from the SPIxSR to the SDOx pin and simultaneously shift in the data at the SDIx pin into the SPIxSR.
4. When the transfer is complete:
 - When the ongoing transmit and receive operation is complete, the contents of the SPIxSR are moved into the next available location in the receive buffer.
 - If the last unread location is written by the SPIx module, the SPIxRBF bit (SPIxSTAT<0>) is set by the module, indicating that all buffer locations are full. SPIx interrupts can be enabled by selecting an interrupt mode with the SISELx bits and setting the SPIx Interrupt Enable bit, SPIxIE. The SPIxIF flag is not cleared automatically by the hardware.
 - Once the SPIxBUF register is read by the user code, the hardware clears the SPIxRBF bit and the SPIxBUF increments to the next unread receive buffer location. SPIxBUF reads beyond the last unread location will not increment the buffer location.
5. If the SPIxRBF bit is set (receive buffer is full) when the SPIx module needs to transfer data from SPIxSR to the buffer, the module will set the SPIROV (SPIxSTAT<6>) bit, indicating an overflow condition and set the SPIxIF bit.
6. Data to be transmitted can be written to SPIxBUF by the user software at any time as long as the SPIxTBF (SPIxSTAT<1>) bit is clear. Up to eight pending transfers can be loaded into the buffer allowing continuous transmission.

The timing of events in Enhanced Buffer Master mode operation is essentially the same as that for Standard Master mode, shown in Figure 23-4.

To set up the SPIx module for the Enhanced Buffer Master mode of operation:

1. If using interrupts:
 - Clear the SPIxIF bit in the respective IFSn register.
 - Select an interrupt mode using the SISELx bits.
 - Set the SPIxIE bit in the respective IECn register.
 - Write the SPIxIP bits in the respective IPCn register.
2. Write the desired settings to the SPIxCON1 and SPIxCON2 registers with the MSTEN bit (SPIxCON1<5>) = 1.
3. Clear the SPIROV bit (SPIxSTAT<6>).
4. Select Enhanced Buffer mode by setting the SPIBEN bit (SPIxCON2<0>).
5. Enable SPIx operation by setting the SPIEN bit (SPIxSTAT<15>).
6. Write the data to be transmitted to the SPIxBUF register. Transmission (and reception) will start as soon as data is written to the SPIxBUF register.

23.3.3.1.1 External Clocking in Master Mode

In Enhanced Buffer Master mode, the module can also be configured to operate with an external data clock. SPIx clock operation is controlled by the DISSCK bit (SPIxCON1<12>). When this bit is set, the internal data clock is disabled and data is transferred when external clock pulses are presented on the SCKx pin. All other aspects of Standard Master mode operation are the same as before.

| |
|--|
| Note: The DISSCK bit is available only in SPI Master modes. |
|--|

23.3.3.2 ENHANCED BUFFER SLAVE MODE

In Slave mode, data is transmitted and received as the external clock pulses appear on the SCKx pin. The CKP (SPIxCON1<6>) and CKE (SPIxCON1<8>) bits determine on which edge of the clock data transmission occurs.

The rest of the operation of the module is identical to that in the Master mode. Specific timings for Enhanced Buffer Slave mode operations are identical to those for Standard Slave mode, as shown in Figure 23-5, Figure 23-6 and Figure 23-7.

To set up the SPIx module for the Enhanced Buffer Slave mode of operation:

1. Clear the SPIxBUF register.
2. If using interrupts:
 - Clear the SPIxIF bit in the respective IFSn register.
 - Select an interrupt mode using the SISELx bits.
 - Set the SPIxIE bit in the respective IECn register.
 - Write the SPIxIP bits in the respective IPCn register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1 and SPIxCON2 registers with the MSTEN bit (SPIxCON1<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit is set, then the SSEN bit must be set, thus enabling the \overline{SSx} pin.
6. Clear the SPIROV bit (SPIxSTAT<6>).
7. Select Enhanced Buffer mode by setting the SPIBEN bit (SPIxCON2<0>).
8. Enable SPIx operation by setting the SPIEN bit (SPIxSTAT<15>).

23.3.3.2.1 Slave Select Synchronization

The \overline{SSx} pin allows a Synchronous Slave mode. If the SSEN (SPIxCON1<7>) bit is set, transmission and reception is enabled in Slave mode only if the \overline{SSx} pin is driven to a low state (see Figure 23-6). The port output or other peripheral outputs must not be driven in order to allow the \overline{SSx} pin to function as an input. If the SSEN bit is set and the \overline{SSx} pin is driven high, the SDOx pin is no longer driven and will tri-state even if the module is in the middle of a transmission. An aborted transmission will be retried the next time the \overline{SSx} pin is driven low using the data held in the SPIxTXB register. If the SSEN bit is not set, the \overline{SSx} pin does not affect the module operation in Slave mode.

Note: To meet module timing requirements, the \overline{SSx} pin must be enabled in Slave mode when CKE = 1 (refer to Figure 23-7 for details).

23.3.3.2.2 SPIxTBF Status Flag Operation

The function of the SPIxTBF bit (SPIxSTAT<1>) is different in the Slave mode of operation. If SSEN is cleared, SPIxTBF is set when the last available buffer location is loaded by the user code. It is cleared when the module transfers data from the buffer to SPIxSR and a buffer location is available for a CPU write. This is similar to the SPIxTBF bit function in Master mode.

If SSEN is set, the SPIxTBF is set when the last available buffer location is loaded by the user code. However, it is cleared only when the SPIx module completes data transmission, leaving a buffer location available for a CPU write. A transmission will be aborted when the \overline{SSx} pin goes high and may be retried at a later time. Each data word is held in the buffer until all bits are transmitted to the receiver.

23.3.4 Framed SPI Modes

The module supports a basic Framed SPI protocol while operating in either Master or Slave modes. The module uses four control bits to configure framed SPI operation:

- FRMEN (SPIxCON2<15>) enables the Framed SPI modes and causes the \overline{SSx} pin to be used as a frame synchronization pulse input or output pin. The state of SSEN (SPIxCON1<7>) is ignored.
- SPIFSD (SPIxCON2<14>) determines whether the \overline{SSx} pin is an input or an output (i.e., whether the module receives or generates the frame synchronization pulse).
- SPIFPOL (SPIxCON2<13>) selects the polarity of the frame synchronization pulse (active-high or active-low) for a single SPIx data frame.
- SPIFE (SPIxCON2<1>) selects the synchronization pulse to either coincide with, or precede, the first serial clock pulse.

The SPIx module supports two Framed modes of operation. In Frame Master mode, the SPIx module generates the frame synchronization pulse and provides this pulse to other devices at the \overline{SSx} pin. In Frame Slave mode, the SPIx module uses a frame synchronization pulse received at the \overline{SSx} pin.

Note: The use of the \overline{SSx} and SCKx pins are mandatory in all Framed SPI modes.

The Framed SPI modes are supported in conjunction with the Unframed Master and Slave modes. This makes four framed SPI configurations available to the user:

- SPI Master mode and Frame Master mode
- SPI Master mode and Frame Slave mode
- SPI Slave mode and Frame Master mode
- SPI Slave mode and Frame Slave mode

These modes determine whether or not the SPIx module generates the serial clock and the frame synchronization pulse.

23.3.4.1 SCKx PIN IN FRAMED SPI MODES

When FRMEN = 1 and MSTEN = 1, the SCKx pin becomes an output and the SPIx clock at SCKx becomes a free-running clock. When FRMEN = 1 and MSTEN = 0, the SCKx pin becomes an input. The source clock provided to the SCKx pin is assumed to be a free-running clock.

The polarity of the clock is selected by the CKP (SPIxCON1<6>) bit. The CKP (SPIxCON1<6>) bit is not used for the Framed SPI modes and should be programmed to '0' by the user software. When CKP = 0, the frame sync pulse output and the SDOx data output change on the rising edge of the clock pulses at the SCKx pin. Input data is sampled at the SDIx input pin on the falling edge of the serial clock. When CKP = 1, the frame sync pulse output and the SDOx data output change on the falling edge of the clock pulses at the SCKx pin. Input data is sampled at the SDIx input pin on the rising edge of the serial clock.

23.3.4.2 SPIx BUFFERS IN FRAMED SPI MODES

When SPIFSD (SPIxCON2<14>) = 0, the SPIx module is in the Frame Master mode of operation. In this mode, the frame sync pulse is initiated by the module when the user software writes the transmit data to the SPIxBUF location (thus writing the SPIxTXB register with transmit data). At the end of the frame sync pulse, the SPIxTXB is transferred to the SPIxSR and data transmission/reception begins.

When SPIFSD = 1, the module is in Frame Slave mode. In this mode, the frame sync pulse is generated by an external source. When the module samples the frame sync pulse, it will transfer the contents of the SPIxTXB register to the SPIxSR and data transmission/reception begins. The user must make sure that the correct data is loaded into the SPIxBUF for transmission before the frame sync pulse is received.

Note: Receiving a frame sync pulse will start a transmission, regardless of whether data was written to SPIxBUF. If no write was performed, the old contents of either SPIxTXB (Standard mode) or the FIFO transmit buffer (Enhanced mode) will be transmitted.

Section 23. Serial Peripheral Interface (SPI)

23.3.4.3 SPI MASTER MODE AND FRAME MASTER MODE

In Master/Frame Master mode, the SPIx module generates both the clock and frame synchronization signals, as shown in Figure 23-9. It is enabled by setting the MSTEN and FRMEN bits to '1' and the SPIFSD bit to '0'.

In this mode, the serial clock is output continuously at the SCKx pin, regardless of whether the module is transmitting. When SPIxBUF is written, the SSx pin will be driven to its active state (as determined by the SPIFPOL bit) on the appropriate transmit edge of the SCKx clock, and remain active for one data frame. If the SPIFE control bit (SPIxCON2<1>) is cleared, the frame sync pulse precedes the data transmission, as shown in Figure 23-10. If SPIFE is set, the frame sync pulse coincides with the beginning of the data transmission, as shown in Figure 23-11. The module starts transmitting data on the next transmit edge of the SCKx.

Figure 23-9: SPI Master, Frame Master Connection Diagram

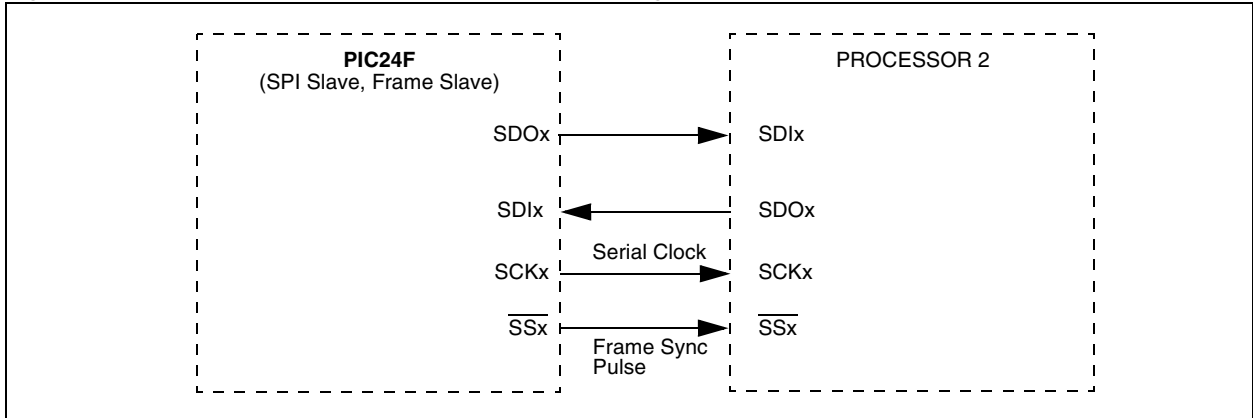


Figure 23-10: SPI Master, Frame Master Timing (SPIFE = 0)

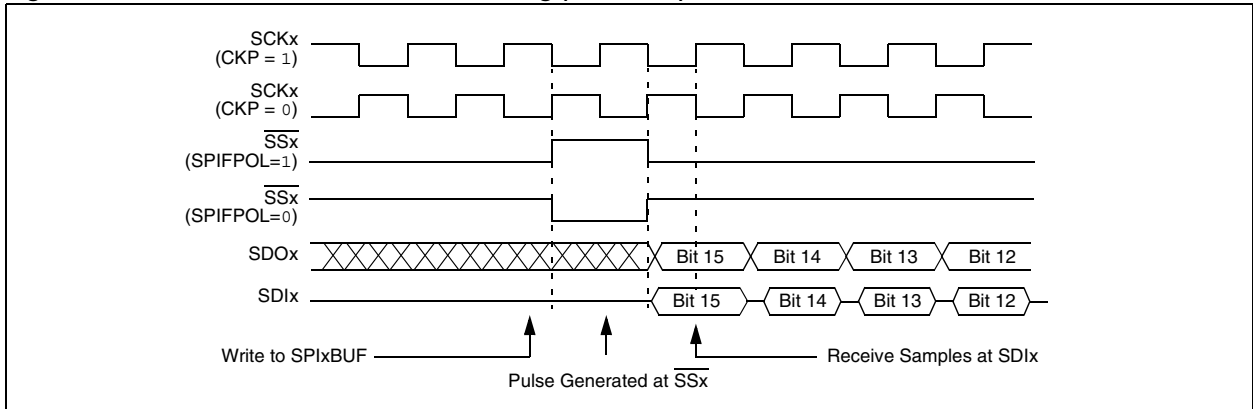
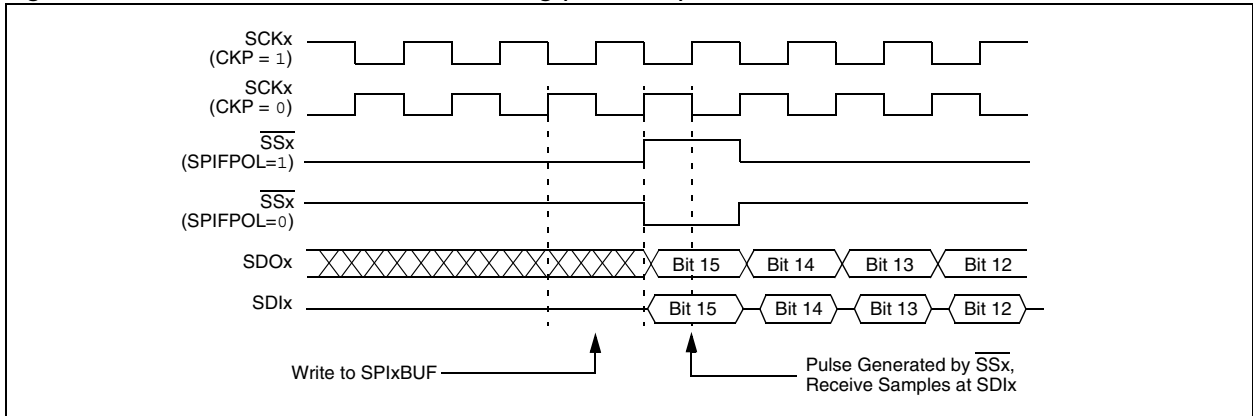


Figure 23-11: SPI Master, Frame Master Timing (SPIFE = 1)



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23.3.4.4 SPI MASTER MODE AND FRAME SLAVE MODE

In Master/Frame Slave mode, the module generates the clock signal but uses the slave module's frame synchronization signal for data transmission (Figure 23-12). It is enabled by setting the MSTEN, FRMEN and the SPIFSD bits to '1'.

In this mode, the \overline{SSx} pin is an input and it is sampled on the sample edge of the SPIx clock. When it is sampled in its active state, data will be transmitted on the subsequent transmit edge of the SPIx clock. The interrupt flag, SPIxIF, is set when the transmission is complete. The user must make sure that the correct data is loaded into the SPIxBUF for transmission before the signal is received at the \overline{SSx} pin.

Figure 23-12: SPI Master, Frame Slave Connection Diagram

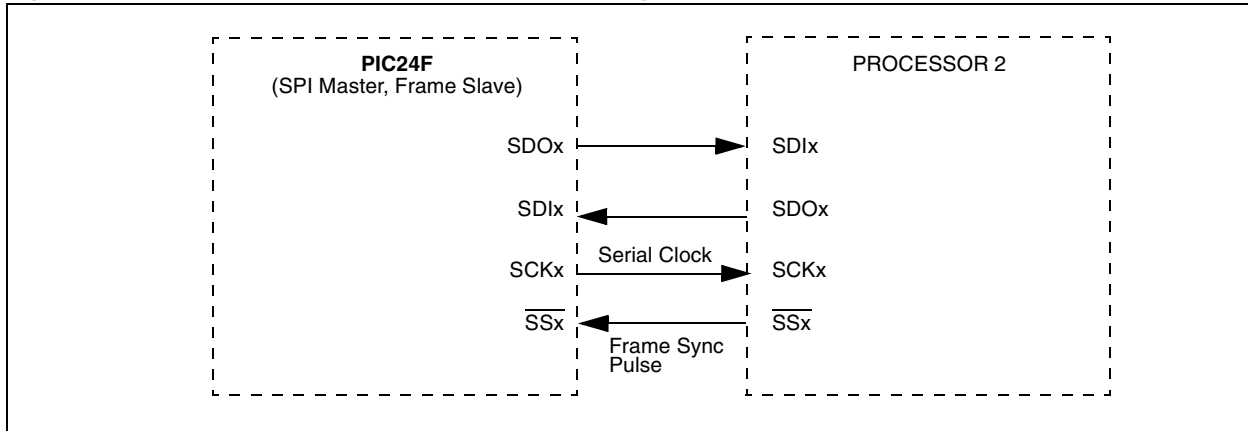


Figure 23-13: SPI Master, Frame Slave Timing (SPIFE = 0)

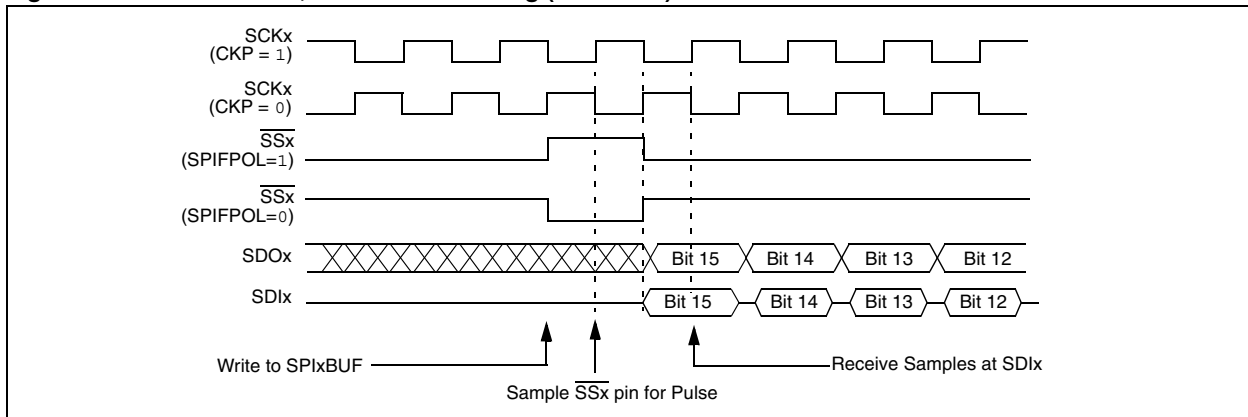
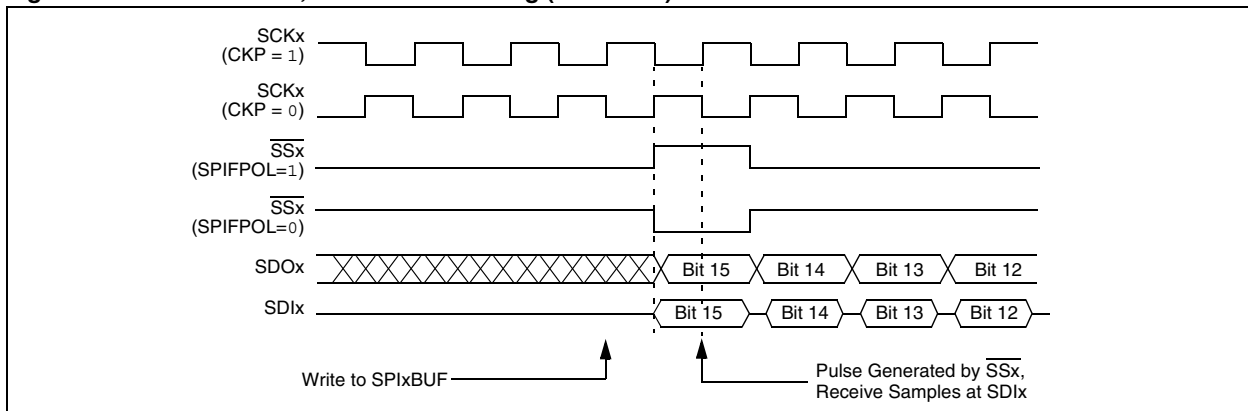


Figure 23-14: SPI Master, Frame Slave Timing (SPIFE = 1)



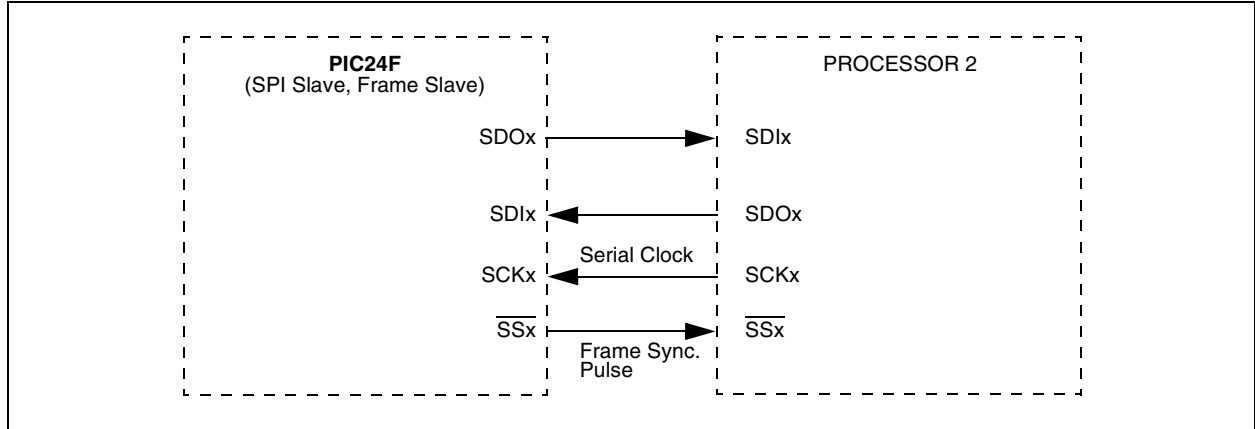
Section 23. Serial Peripheral Interface (SPI)

23.3.4.5 SPI SLAVE MODE AND FRAME MASTER MODE

In Slave/Frame Master mode, the module acts as the SPI slave and takes its clock from the other SPI module; however, it produces frame synchronization signals to control data transmission (Figure 23-15). It is enabled by setting the MSTEN bit to '0', the FRMEN bit to '1' and the SPIFSD bit to '0'.

The input SPIx clock will be continuous in Slave mode. The \overline{SSx} pin will be an output when the SPIFSD bit is low. Therefore, when the SPIxBUF is written, the module drives the \overline{SSx} pin to the active state on the appropriate transmit edge of the SPIx clock for one SPIx clock cycle. Data will start transmitting on the appropriate SPIx clock transmit edge.

Figure 23-15: SPI Slave, Frame Master Connection Diagram

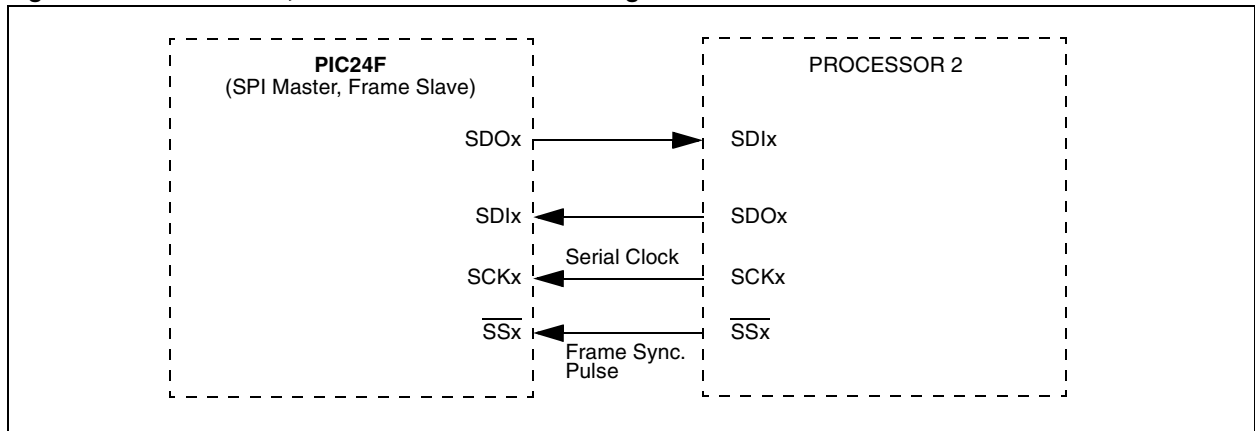


23.3.4.6 SPI SLAVE MODE AND FRAME SLAVE MODE

In Slave/Frame Slave mode, the module obtains both its clock and frame synchronization signal from the master module (Figure 23-16). It is enabled by setting MSTEN to '0', FRMEN to '1' and SPIFSD to '1'.

In this mode, both the SCKx and \overline{SSx} pins will be inputs. The \overline{SSx} pin is sampled on the sample edge of the SPIx clock. When \overline{SSx} is sampled at its active state, data will be transmitted on the appropriate transmit edge of SCKx.

Figure 23-16: SPI Slave, Frame Slave Connection Diagram



23.3.5 SPIx Receive Only Operation

Setting the DISSDO control bit (SPIxCON1<11>) disables transmission at the SDOx pin. This allows the SPIx module to be configured for a Receive Only mode of operation. The SDOx pin will be controlled by the respective port function if the DISSDO bit is set.

The DISSDO function is applicable to all SPIx operating modes.

23.3.6 SPIx Error Handling

If a new data word has been shifted from the SPIx bus into SPIxSR, and no more unread buffer locations are available, the SPIROV bit (SPIxSTAT<6>) will be set. Any received data in SPIxSR will not be transferred and further data reception is disabled until the SPIROV bit is cleared. The SPIROV bit is not cleared automatically by the module; it must be cleared by the user software.

The SPIx Interrupt Flag, SPFxIF, is set whenever the SPIROV, SPIxRBF (SPIxSTAT<0>) or SPIxTBF (SPIxSTAT<1>) bits are set. The interrupt flag cannot be cleared by hardware and must be reset in software. The actual SPIx interrupt is generated only when the corresponding SPFxIE bit is set in the IECn Control register

23.4 SPI MASTER MODE CLOCK FREQUENCY

In the Master mode, the clock provided to the SPIx module is the instruction cycle (Tcy). This clock will then be prescaled by the primary prescaler, specified by the PPRE1:PPRE0 bits (SPIxCON1<1:0>) and the secondary prescaler, specified by the SPRE2:SPRE0 bits (SPIxCON1<4:2>). The prescaled instruction clock becomes the serial clock and is provided to external devices via the SCKx pin.

Note: Note that the SCKx signal clock is not free running for normal SPI modes. It will only run for 8 or 16 pulses when the SPIxBUF is loaded with data. It will, however, be continuous for Framed modes.

Equation 23-1 can be used to calculate the SCKx clock frequency as a function of the primary and secondary prescaler settings.

Equation 23-1:

$$F_{SCK} = \frac{F_{CY}}{\text{Primary Prescaler} * \text{Secondary Prescaler}}$$

Some sample SPIx clock frequencies (in kHz) are shown in Table 23-2:

Table 23-1: Sample SCK Frequencies^(1,2)

| Fcy = 16 MHz | | Secondary Prescaler Settings | | | | |
|----------------------------|------|------------------------------|------|------|------|------|
| | | 1:1 | 2:1 | 4:1 | 6:1 | 8:1 |
| Primary Prescaler Settings | 1:1 | (Invalid) | 8000 | 4000 | 2667 | 2000 |
| | 4:1 | 4000 | 2000 | 1000 | 667 | 500 |
| | 16:1 | 1000 | 500 | 250 | 167 | 125 |
| | 64:1 | 250 | 125 | 63 | 42 | 31 |
| Fcy = 5 MHz | | | | | | |
| Primary Prescaler Settings | 1:1 | 5000 | 2500 | 1250 | 833 | 625 |
| | 4:1 | 1250 | 625 | 313 | 208 | 156 |
| | 16:1 | 313 | 156 | 78 | 52 | 39 |
| | 64:1 | 78 | 39 | 20 | 13 | 10 |

Note 1: Based on Tcy = TOSC/2; Doze mode and PLL are disabled.

2: SCKx frequencies shown in kHz.

Note: Not all clock rates are supported. For further information, refer to the SPIx timing specifications in the specific device data sheet.

23.5 OPERATION IN POWER-SAVING MODES

The PIC24 family of devices has three Power modes: the normal Operational (Full-Power) mode, and the two Power-Saving modes, invoked by the `PWRSSAV` instruction. Depending on the SPI mode selected, entering a Power-Saving mode may also affect the operation of the module.

23.5.1 Sleep Mode

When the device enters Sleep mode, the system clock is disabled. The consequences of entering Sleep depend on which mode (Master or Slave) the module is configured in at the time that Sleep mode is invoked.

23.5.1.1 MASTER MODE OPERATION

The following are a consequence of entering Sleep mode when the SPIx module is configured for master operation:

- The Baud Rate Generator in the SPIx module stops and is reset.
- The transmitter and receiver will stop in Sleep. The transmitter or receiver will not continue with a partially completed transmission at wake-up.
- If the SPIx module enters Sleep mode in the middle of a transmission or reception, the transmission or reception is aborted. Since there is no automatic way to prevent an entry into Sleep mode if a transmission or reception is pending, the user software must synchronize entry into Sleep with the SPIx module operation to avoid aborted transmissions.

23.5.1.2 SLAVE MODE OPERATION

Since the clock pulses at SCKx are externally provided for Slave mode, the module will continue to function in Sleep mode. It will complete any transactions during the transition into Sleep. On completion of a transaction, the SPIxRBF flag is set. Consequently, the SPIxIF bit will be set. If SPIx interrupts are enabled (SPIxIE = 1), the device will wake from Sleep. If the SPIx interrupt priority level is greater than the present CPU priority level, code execution will resume at the SPIx interrupt vector location. Otherwise, code execution will continue with the instruction following the `PWRSSAV` instruction that previously invoked Sleep mode. The module is not reset on entering Sleep mode if it is operating as a slave device.

Register contents are not affected when the SPIx module is going into or coming out of Sleep mode.

23.5.2 Idle Mode

When the device enters Idle mode, the system clock sources remain functional. The SPISIDL bit (SPIxSTAT<13>) selects whether the module will stop or continue functioning on Idle.

If SPISIDL = 1, the SPIx module will stop communication on entering Idle mode. It will operate in the same manner as it does in Sleep mode. If SPISIDL = 0 (default selection), the module will continue operation in Idle mode.

23.6 REGISTER MAPS

A summary of the registers associated with the PIC24F family SPIx module is provided in Table 23-2.

Table 23-2: SPIx Memory Map

| Name | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|----------------------------------|--------|--------|---------|--------|--------|---------|---------|---------|--------|--------|--------|--------|--------|--------|---------|---------|------------|
| SPIxSTAT | SPIEN | — | SPIIDL | — | — | SPIBEC2 | SPIBEC1 | SPIBEC0 | SRMPT | SPIROV | SRXMPT | SISEL2 | SISEL1 | SISEL0 | SPIxTBF | SPIxRBF | 0000 |
| SPIxCON1 | — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | SPRE2 | SPRE1 | SPRE0 | PPRE1 | PPRE0 | 0000 |
| SPIxCON2 | FRMEN | SPIFSD | SPIFPOL | — | — | — | — | — | — | — | — | — | — | — | SPIFE | SPIBEN | 0000 |
| SPIx Transmit and Receive Buffer | | | | | | | | | | | | | | | | | |
| SPIxBUF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| PMD1 | T5MD | T4MD | T3MD | T2MD | T1MD | — | — | — | I2C1MD | U2MD | U1MD | SP12MD | SP11MD | — | — | ADCMD | 0000 |
| PMD2 | — | — | — | IC5MD | IC4MD | IC3MD | IC2MD | IC1MD | — | — | — | OC5MD | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | — | — | — | — | — | CMPMD | RTCCMD | PMPMD | CRCPMD | — | — | — | — | — | I2CMD | — | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

23.7 ELECTRICAL SPECIFICATIONS

Figure 23-17: SPIx Module Master Mode Timing Characteristics (CKE = 0)

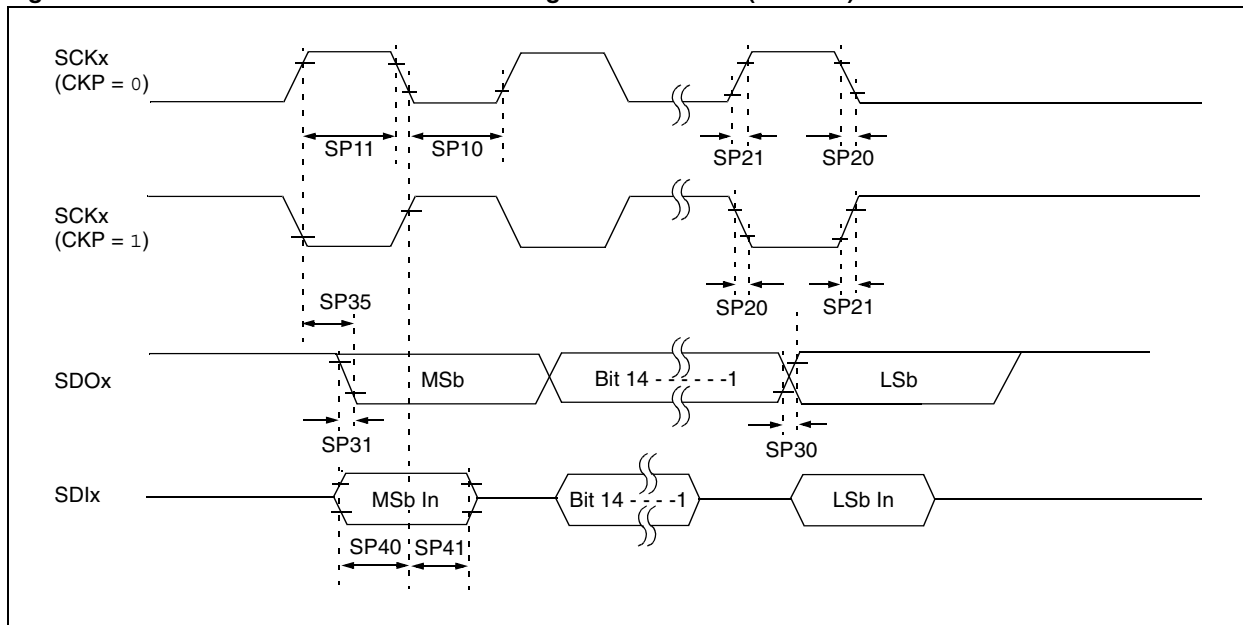


Table 23-3: SPIx Master Mode Timing Requirements (CKE = 0)

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial | | | | |
|--------------------|-----------------------|--|--|--------------------|-----|-------|------------|
| Param No. | Symbol | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| SP10 | TscL | SCKx Output Low Time ⁽²⁾ | $T_{CY}/2$ | — | — | ns | |
| SP11 | TscH | SCKx Output High Time ⁽²⁾ | $T_{CY}/2$ | — | — | ns | |
| SP20 | TscF | SCKx Output Fall Time ⁽³⁾ | — | 10 | 25 | ns | |
| SP21 | TscR | SCKx Output Rise Time ⁽³⁾ | — | 10 | 25 | ns | |
| SP30 | TdoF | SDOx Data Output Fall Time ⁽³⁾ | — | 10 | 25 | ns | |
| SP31 | TdoR | SDOx Data Output Rise Time ⁽³⁾ | — | 10 | 25 | ns | |
| SP35 | Tsch2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 30 | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 20 | — | — | ns | |
| SP41 | Tsch2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 20 | — | — | ns | |

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

Note 2: The minimum clock period for SCKx is 100 ns; therefore, the clock generated in Master mode must not violate this specification.

Note 3: Assumes 50 pF load on all SPIx pins.

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Figure 23-18: SPIx Module Master Mode Timing Characteristics (CKE = 1)

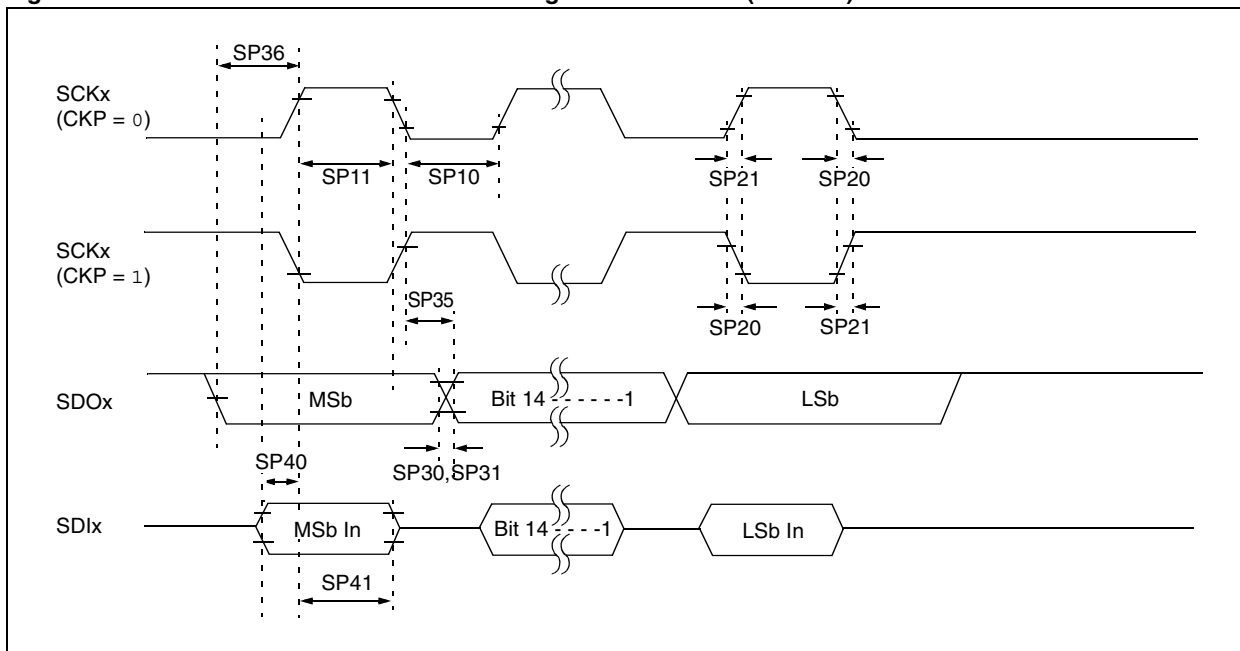


Table 23-4: SPIx Module Master Mode Timing Requirements (CKE = 1)

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial | | | | |
|--------------------|-----------------------|--|--|--------------------|-----|-------|------------|
| Param No. | Symbol | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| SP10 | TscL | SCKx Output Low Time ⁽²⁾ | $T_{CY}/2$ | — | — | ns | |
| SP11 | Tsch | SCKx Output High Time ⁽²⁾ | $T_{CY}/2$ | — | — | ns | |
| SP20 | TscF | SCKx Output Fall Time ⁽³⁾ | — | 10 | 25 | ns | |
| SP21 | TscR | SCKx Output Rise Time ⁽³⁾ | — | 10 | 25 | ns | |
| SP30 | TdoF | SDOx Data Output Fall Time ⁽³⁾ | — | 10 | 25 | ns | |
| SP31 | TdoR | SDOx Data Output Rise Time ⁽³⁾ | — | 10 | 25 | ns | |
| SP35 | Tsch2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 30 | ns | |
| SP36 | TdoV2sc, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2sch, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 20 | — | — | ns | |
| SP41 | Tsch2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 20 | — | — | ns | |

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

3: Assumes 50 pF load on all SPIx pins.

Section 23. Serial Peripheral Interface (SPI)

Figure 23-19: SPIx Module Slave Mode Timing Characteristics (CKE = 0)

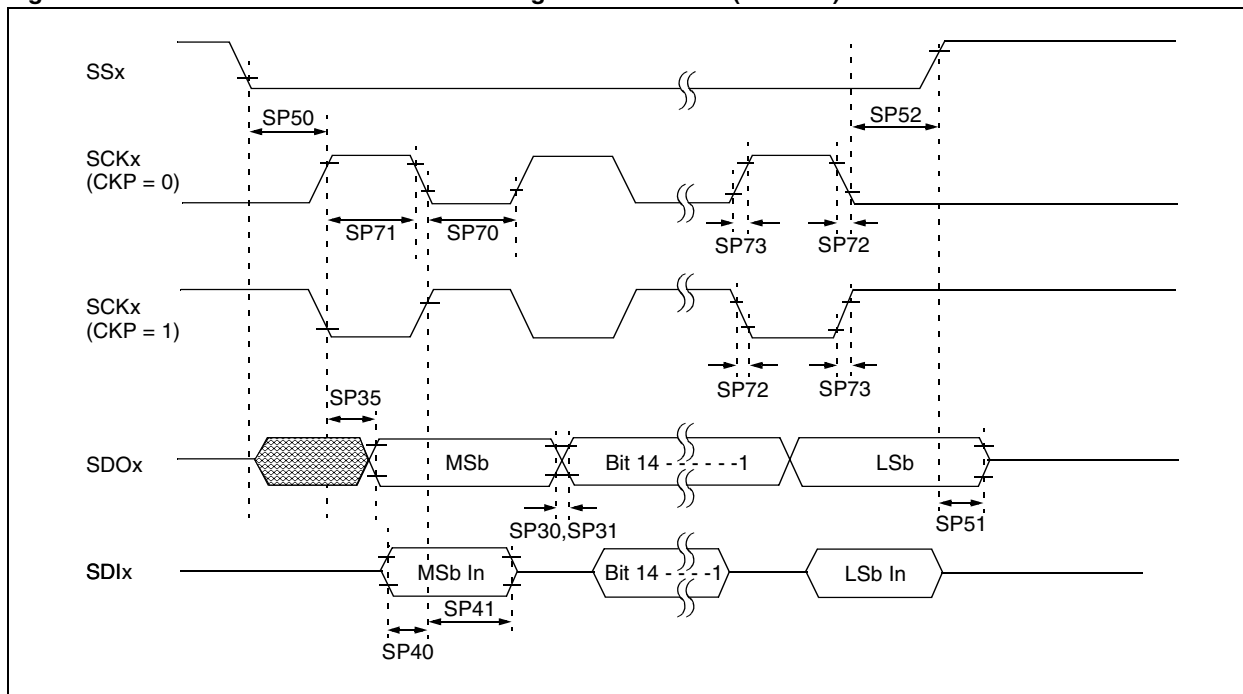


Table 23-5: SPIx Module Slave Mode Timing Requirements (CKE = 0)

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial | | | | |
|--------------------|-----------------------|---|--|--------------------|-----|-------|------------|
| Param No. | Symbol | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| SP70 | TscL | SCKx Input Low Time | 30 | — | — | ns | |
| SP71 | TschH | SCKx Input High Time | 30 | — | — | ns | |
| SP72 | TscF | SCKx Input Fall Time ⁽²⁾ | — | 10 | 25 | ns | |
| SP73 | TscR | SCKx Input Rise Time ⁽²⁾ | — | 10 | 25 | ns | |
| SP30 | TdoF | SDOx Data Output Fall Time ⁽²⁾ | — | 10 | 25 | ns | |
| SP31 | TdoR | SDOx Data Output Rise Time ⁽²⁾ | — | 10 | 25 | ns | |
| SP35 | Tsch2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 30 | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 20 | — | — | ns | |
| SP41 | Tsch2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 20 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{\text{SSx}}$ to SCKx \uparrow or SCKx Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{\text{SSx}}$ \uparrow to SDOx Output High-Impedance ⁽³⁾ | 10 | — | 50 | ns | |
| SP52 | Tsch2ssh, TscL2ssh | $\overline{\text{SSx}}$ after SCKx Edge | $1.5 T_{CY} + 40$ | — | — | ns | |

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Assumes 50 pF load on all SPIx pins.

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Figure 23-20: SPIx Module Slave Mode Timing Characteristics (CKE = 1)

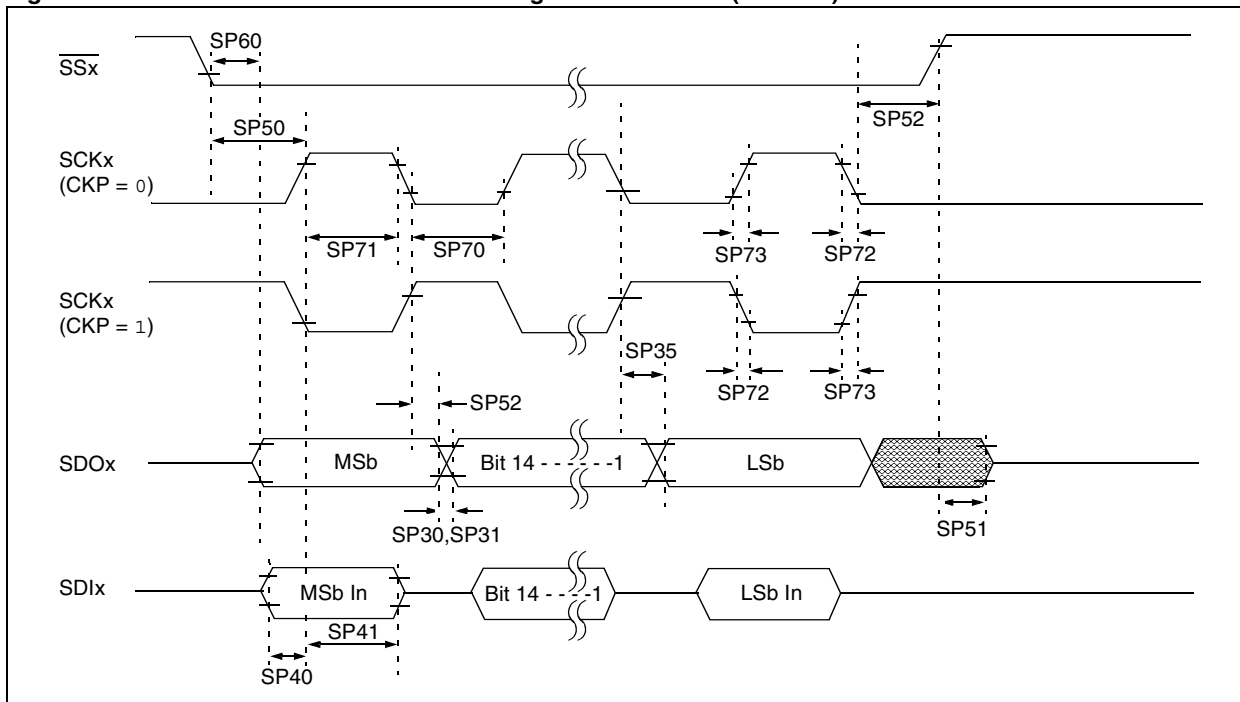


Table 23-6: SPIx Module Slave Mode Timing Requirements (CKE = 1)

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial | | | | |
|--------------------|-----------------------|--|--|--------------------|-----|-------|------------|
| Param No. | Symbol | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| SP70 | TscL | SCKx Input Low Time | 30 | — | — | ns | |
| SP71 | Tsch | SCKx Input High Time | 30 | — | — | ns | |
| SP72 | TscF | SCKx Input Fall Time ⁽²⁾ | — | 10 | 25 | ns | |
| SP73 | TscR | SCKx Input Rise Time ⁽²⁾ | — | 10 | 25 | ns | |
| SP30 | TdoF | SDOx Data Output Fall Time ⁽²⁾ | — | 10 | 25 | ns | |
| SP31 | TdoR | SDOx Data Output Rise Time ⁽²⁾ | — | 10 | 25 | ns | |
| SP35 | Tsch2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 30 | ns | |
| SP40 | TdiV2sch, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 20 | — | — | ns | |
| SP41 | Tsch2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 20 | — | — | ns | |
| SP50 | TssL2sch, TssL2scL | $\overline{\text{SSx}} \downarrow$ to SCKx \downarrow or SCKx \uparrow Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{\text{SSx}} \uparrow$ to SDOx Output High-Impedance ⁽³⁾ | 10 | — | 50 | ns | |
| SP52 | Tsch2ssH TscL2ssH | $\overline{\text{SSx}} \uparrow$ after SCKx Edge | $1.5 T_{CY} + 40$ | — | — | ns | |
| SP60 | TssL2doV | SDOx Data Output Valid after $\overline{\text{SSx}}$ Edge | — | — | 50 | ns | |

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

Note 2: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

Note 3: Assumes 50 pF load on all SPIx pins.

23.8 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Serial Peripheral Interface (SPI) module are:

| Title | Application Note # |
|---|--------------------|
| Interfacing Microchip's MCP41XXX and MCP42XXX Digital Potentiometers to a PICmicro® Microcontroller | AN746 |
| Interfacing Microchip's MCP3201 Analog-to-Digital Converter to the PICmicro® Microcontroller | AN719 |

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

23.9 REVISION HISTORY

Revision A (August 2006)

This is the initial released revision of this document.

Revision B (March 2007)

Added FIFO functionality.

Section 23. Serial Peripheral Interface (SPI)

NOTES:

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Serial Peripheral
Interface (SPI)